IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Paul M. Henry	Examiner:	Terry D. Cunningham
Application No.:	10/651,849	Group Art Unit:	2816
Filed:	August 29, 2003	Docket No.:	50019.242US01/P05640
Title:	NULLED ERROR AMPLIFIER		

CERTIFICATE UNDER 37 CFR 1.10:
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Date of Deposit: March 24, 2006
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By: _____
Name: Alice Baum

DECLARATION UNDER 37 C.F.R. § 1.132

I, Paul M. Henry, am a citizen of the United States of America, and a resident of the state of Arizona, declare:

1. I am the sole inventor of the subject matter claimed in U.S. Patent Application No. 10/651,849), filed August 29, 2003, and entitled "NULLED ERROR AMPLIFIER."

2. The terms “band-gap”, “band-gap core”, “band-gap core circuit”, and “band-gap circuit” that appear in Applicant’s claims and specification have a specific meaning that is understood to one of ordinary skill in the relevant art. As is understood in the art, the accepted meaning of the terms “band-gap”, “band-gap core”, “band-gap core circuit”, and “band-gap circuit” require that every such described device must necessarily include two bipolar junction transistors (BJTs) and a resistor in a specific configuration. The specific configuration imparted to the term “band-gap” is understood to include a common-base configuration for the two BJTs, where the first bipolar junction transistor has a first operational base-emitter voltage (VBE1), and the second bipolar junction transistor has a second operational base-emitter voltage (VBE2). The specific

configuration imparted to the term "band-gap" is also understood to include that a voltage appears across the resistor corresponding to delta VBE. It is further understood in the art that the term "band-gap" does not have any relevant meaning without requiring closed-loop feedback operation such that VBE1 = VBE2 + delta VBE.

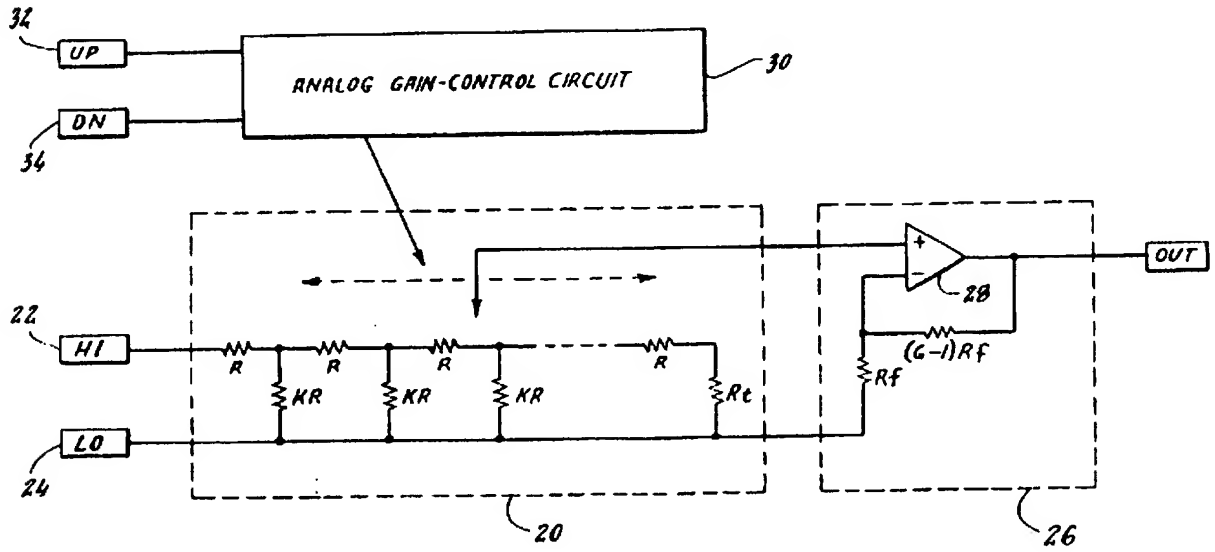
3. The above described interpretation of the terms "band-gap", "band-gap core", "band-gap core circuit", and "band-gap circuit" are supported by objective evidence that is presented in the form of an information disclosure statement. Objective evidence is found with reference to Figs. 11.30 and 11.33, and the supporting text on pages 397 and 399 of "Design of Analog CMOS Integrated Circuits" by Behzad Razavi, where the terms "band-gap" and "core" are specifically used together in proper context and consistent with the Applicant's intended meaning. Further objective evidence is found with reference to Fig. 3 and the supporting text on page 2 of "A Low Voltage Bandgap Reference Circuit with Current Feedback" by Li, Mitra and Udeshi, wherein the terms "band-gap" and "core" are again specifically used together in proper context and consistent with the Applicant's intended meaning. Still further objective evidence is found with reference to Figs. 2 and 4, and the supporting text on pages 3 and 6 of "Predicting and Designing for the Impact of Process Variations and Mismatch on the Trim Range and Yield of Bandgap References" by Gupta and Rincon-Mora, wherein the terms "band-gap" and "core" are still again specifically used together in proper context and consistent with the Applicant's intended meaning.

4. Applicant has thoroughly reviewed U.S. Patent No. 5,077,541 to *Gilbert*. Nothing in the *Gilbert* reference provides any explicit or implicit support for any variety of "band-gap" circuit as is understood in the art. Applicant has reviewed the detailed description of *Gilbert* and finds

no explicit reference for the term "band-gap" or any equivalent terms. Applicant has also reviewed the detailed description and the drawings of *Gilbert* and does not find any inherent support for a "band-gap" or any functional or structural equivalent as is understood in the art. The principals of operation taught in the *Gilbert* reference are incompatible with the functional and/or structural criteria necessary for a "band-gap".

5. Objective evidence of the incompatibility of the *Gilbert* reference with any variety of "band-gap" operation is found in the *Gilbert* reference itself. FIG. 1 of *Gilbert* illustrates the principal of operation along with the supporting text from col. 3, lines 1 – 25, where an input signal is applied at terminals 22 and 24 to a resistive attenuator 20.

Fig. 1.

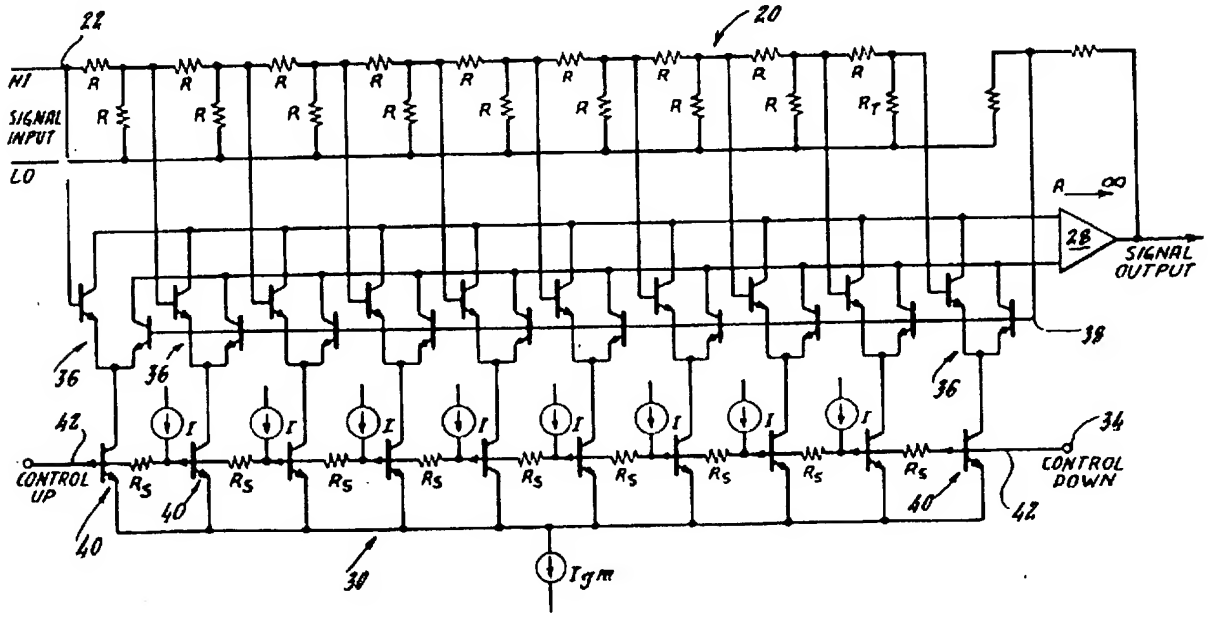


Since terminal 24 is connected to a low impedance voltage source, ideally zero ohms, terminal 24 is a ground terminal and no feedback signal is present at terminal 24. The office action of January 27, 2006 states that *Gilbert* describes "a feedback means (feedback resistor, R,

RT and resistor between 38 and RT)", and that "since the feedback arrangement would provide a band-gap operation, it would have been more than reasonable to consider the feedback means to be a "band-gap core circuit". Resistor RT in FIG. 1 is coupled to the ground provided by terminal 24, as is resistor RF. It is clear that a ground terminal cannot provide feedback. Moreover, the feedback operation of resistors RF and (G-1)RF are a classic non-inverting gain amplifier which by definition cannot be a band-gap variety of circuit. Instead, resistors RF and (G-1)RF are referred to as gain setting resistors for the non-inverting amplifier.

The resistor that is between 38 and resistor RT of Gilbert in Fig. 3 corresponds to the very same resistor illustrated as resistor RF for Fig. 1.

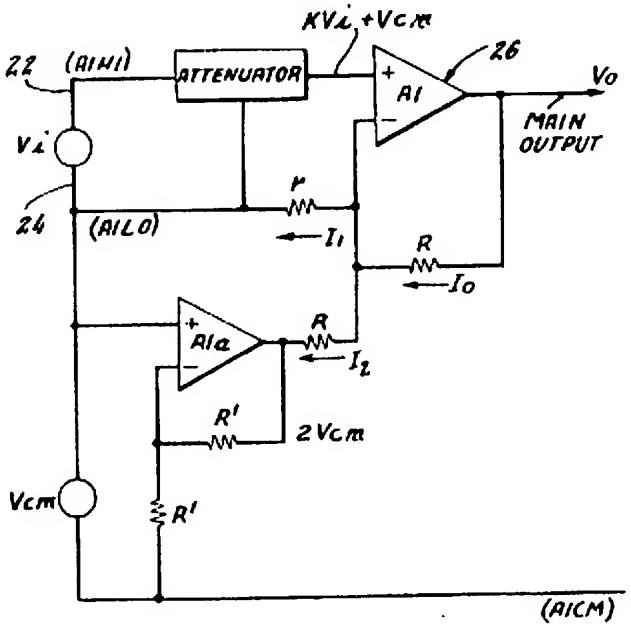
Fig. 3



The resistor between 38 and resistor RT is connected to terminal LO, which as illustrated previously is a voltage source input terminal that acts as a signal ground for any current that is provided from the output of amplifier 28.

The described operation above is further illustrated in Fig. 12 of Gilbert, which is a schematic that provides a technical analysis of operation for the teachings of the patent. The resistor ladder from Fig. 3 of *Gilbert* is illustrated as a block labeled "attenuator".

Fig. 12.



It is important to notice in FIG. 12 that terminal 24 is connected to a DC voltage source VCM, and the input signal VI is referenced with respect to terminal 24. Therefore, the voltage associated with terminal 24 is a static value. Terminal 24 has the exact same functional features as the LO terminal from FIGS. 1-3 of *Gilbert*. Since it is well understood in the art that voltage

sources ideally have zero input impedance, the suggested resistors "(feedback resistor, R, RT and resistor between 38 and RT)" cannot provide feedback operation as a "band-gap" as is suggested in the Office Action.

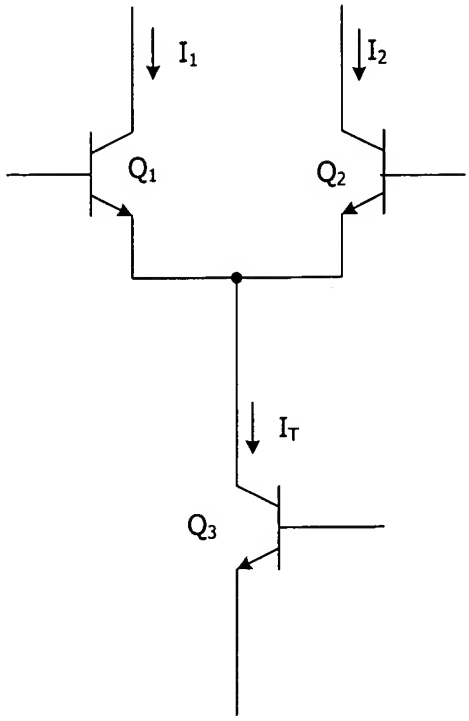
6. The terms "null", "zero", "nulling", and "zeroing" that appear in Applicant's claims and specification have a specific meaning within the context of amplifier offsets that is understood to one of ordinary skill in the relevant art. As is understood in the art, amplifiers have an inherent input referred offset. It is further understood in the art that the terms "null", "zero", "nulling", and "zeroing" are referred to for the process, methods, and devices that are used to calibrate or remove such input referred offset from an amplifier. It is also well understood in the art that amplifier circuits must be active during the calibration or removal of such input referred offset.

7. The above described interpretation of the terms "null", "zero", "nulling", and "zeroing" within the context of amplifiers with "offset" are supported by objective evidence that is presented in the form of an information disclosure statement. Objective evidence is found with reference to U.S. Patent No. 5,847,670 to *Gratrex* et al. where the terms "offset" and "nulling" are specifically used together in proper context and consistent with the Applicant's intended meaning. Specifically, the phrase "offset nulling" is used in *Gratex* at col. 1, lines 15-20 to mean "offset voltage compensation". Further objective evidence is found with reference to an online dictionary at the "answers.com" website, which defines the term "offset null" as "an op amp control pin used to eliminate the effects of internal component voltages on the output of the device." Still further objective evidence is found with reference to pages 374 – 375 of "BIPOLAR AND MOS ANALOG CIRCUIT DESIGN" by Grebene, wherein the terms "offset nulling", "zero", "auto-zero" are specifically used together in proper context and consistent with

the Applicant's intended meaning of removing offset voltage from the input of the amplifier. It is also readily apparent from the above objective evidence that offset removal, cancellation, zeroing, nulling operations can only be accomplished by measuring the input referred offsets when the amplifier is active.

8. Applicant has again thoroughly reviewed U.S. Patent No. 5,077,541 to *Gilbert*. Nothing in the *Gilbert* reference provides any explicit or implicit support for any variety of "offset nulling" as is understood in the art. Applicant has reviewed the detailed description of *Gilbert* and finds no explicit reference to the terms "null", "nulling", "zero", "zeroing", "autozero", and "autozeroing", "offset removal", "offset canceling", "offset zeroing", "offset nulling" and other equivalent terms and phrases. Applicant has also reviewed the detailed description and the drawings of *Gilbert* and does not find any inherent support for a "offset nulling" or any functional or structural equivalent as is understood in the art. The principals of operation taught in the *Gilbert* reference are incompatible with the functional and/or structural criteria necessary for a "band-gap".

9. Objective evidence of the incompatibility of the *Gilbert* reference with any variety of "offset nulling" operation is found in the *Gilbert* reference itself, as well as pages 224 – 228 of "BIPOLAR AND MOS ANALOG INTEGRATERD CIRCUIT DESIGN" by *Grebene*. Integrated circuit amplifier's have an input referred offset voltage that is the result of various device mismatches. The analysis of offset voltages provided below is consistent with the above identified reference, and clearly establishes the operational features of the gm stages in *Gilbert*.



Transistors Q_1 and Q_2 form a differential pair with a common emitter connection. The common emitter connection is connected to the collector of transistor Q_3, which is biased for operation as a current source to provide current I_T. When transistors Q_1 and Q_2 are perfectly matched, and they are operated with identical input signals at their respective bases, there in no input referred offset for the amplifier. In other words, equally applied signals at the base of transistors Q_1 and Q_2 result in perfectly matched currents for I_1 and I_2, where $I_1 = I_2 = I_T/2$. An input referred offset occurs in this amplifier circuit when there is a mismatch between the emitter areas of transistors Q_1 and Q_2, or some other similar process derived mismatch.

A mismatch between transistors Q_1 and Q_2 yields a difference in the currents I1 and I2, which are ideally matched when there is no offset in circuit. In this case, an additional biasing voltage will need to be applied to one of the transistors to match currents I_1 and I_2. The

additional voltage that needs to be applied to the transistors is referred to as the input referred offset, which is a well understood and accepted term in the art. For a 10% mismatch in currents, and equal base voltages applied to Q_1 and Q_2, $I_1 = (1.1)\ I_2$ and is given as:

$$I_1 = I_{S_1} e^{V_{BE_1}/V_{TH}}$$
$$I_2 = 1.1 I_{S_1} e^{V_{BE_2}/V_{TH}}$$

The voltage that needs to be applied between the inputs to match current I_1 to current I_2 is the offset voltage, which is given as $V_{OS} = V_{BE1} - V_{BE2}$. Dividing the above equations results in the following:

$$\frac{I_1}{I_2} = \frac{I_{S_1}}{1.1 I_{S_1}} e^{(V_{BE_1} - V_{BE_2})/V_{TH}}$$

When $V_{BE1} - V_{BE2} = V_{OS}$, currents I_1 and I_2 are matched ($I_1 = I_2$), yielding:

$$1.1 = e^{V_{OS}/V_{TH}}$$

Taking the natural log of both sides and rearranging the equations yields the following:

$$V_{OS} = V_{TH} \ln(1.1) = .026(.0953) = 2.47mV$$

In the above described example the offset voltage V_{OS}, is given as V_{TH} ln(1.1). However, the key observation is that the offset voltage (V_{OS}) is independent of the biasing current I_T.

Instead, as illustrated by the above mathematical relationships, offset voltage is related to the current mismatch ratio (e.g., 1.1 for a 10% mismatch in the above example) and the thermal voltage (kT/q), both of which are independent of the current (I_T) provided by transistor Q_3. Thus, changing the bias current to the differential pair by adjusting the biasing of transistor Q_3 is not useful to adjust the offset voltage.

Referring to at least Fig. 3 of Gilbert, we can observe that each gm stage (36) includes two transistors that are arranged as a differential pair, meaning that they have common-emitter connections with different base connections. The tail current source for this differential pair is represented as transistor 40. The bias current to transistor 40 in Figs. 3 and 4 of Gilbert is provided in part by current source I, and in part by any additional biasing current provided through resistor R_S. By varying the UP and DOWN control signals the total biasing current to transistor 40. Varying the biasing current to transistor 40 has the effect of varying the tail current (e.g. I_T) to the differential pair. However, varying the biasing current to a differential pair has no effect on the offset voltage as a consequence of the inherent characteristics of BJT based differential pairs (see above analysis). In sum, varying the UP and DOWN control signals cannot be used to provide a deterministic effect on the offset voltage.

The Office Action states that Gilbert teaches that each amplifier circuit includes "an offset adjustment circuit (I)" in Figs. 3 and 4 that are arranged in accordance with Applicant's claims. For the above stated reasons, it is clear that adjustment of the current I does not yield any deterministic adjustment to offset voltage on the differential pair. Likewise, adjustment of the UP and DOWN control signals of *Gilbert* yields no deterministic adjustment to offset voltage.

10. I, the undersigned inventor, declare that all statements herein made of my own knowledge are true and that all statements are made on information and belief and are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine and/or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statement may jeopardize the validity of this application or any patent resulting therefrom.

_____
Date

_____
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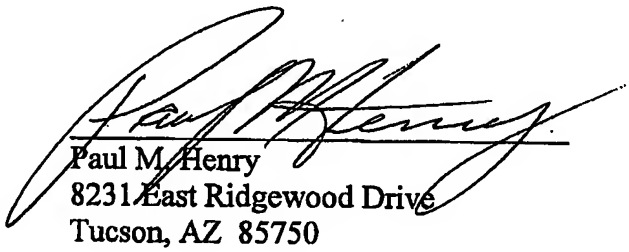
24 March 2006
Date



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